EXHIBIT 4

EXHIBIT C2

Invalidity of U.S. Patent No. 11,093,417 in View of U.S. Patent No. 7,103,742 B1 (*Mailloux*)

U.S. Patent No. 7,103,742 B1 to Mailloux et al. ("*Mailloux*"), filed on December 3, 1997 and issued on September 5, 2006, qualifies as prior art under at least 35 U.S.C. §§ 102 and/or 103 for the asserted claims of U.S. Patent No. 11,093,417 ("the '417 patent"), as discussed in detail in the claim chart below.

The Court has not yet construed the claims and therefore the meaning of the terms in the claims has yet to be resolved by the Court. The support identified here for this limitation is responsive to Plaintiff's infringement contentions, which Defendants disagree with. As such, nothing in Defendants' claim charts should be construed as an admission regarding infringement, either literally or under the doctrine of equivalents, or as an admission regarding Defendants' understanding of the proper scope of the asserted claims. Defendants reserve the right to rely on additional citations or sources of evidence that also may be applicable, or that may become applicable in light of claim construction, changes in Netlist's infringement contentions, and/or information obtained during discovery as the case progresses.

To the extent Netlist alleges that *Mailloux* does not disclose any particular limitation of the asserted claims of the '417 patent, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the priority date of the '417 patent to modify *Mailloux* and/or to combine the teachings of *Mailloux* with other prior art references, including but not limited to the present prior art references cited in the Cover Pleading and the relevant section(s) of claim charts for other prior art references for the '417 patent in a manner that would have rendered the asserted claims invalid as obvious.

Defendants reserve the right to amend or supplement this claim chart at a later date as more fully set forth in the Cover Pleading.

EXHIBIT C2

Invalidity of U.S. Patent No. 11,093,417 in View of U.S. Patent No. 7,103,742 B1 (*Mailloux*)

'417 Patent	**U.S. Patent No. 7,103,742 B1 (*Mailloux*)**
	understood, as illustratively shown in FIG. 9, that memory array 111 may be made up of one or more addressable memory arrays. Memory 100 may provide an output read from memory array 111 via data (DQ) signal 116. Alternatively, memory 100 is capable of receiving information to be stored in memory array 111 via DQ signal 116. DQ signal 116 is made up of I/O pins DQ 1 through DQm inclusive (DQ1—DQm), where m represents an integer greater than or equal to one. Alternatively, separate data input and output paths may be used." *Mailloux* at 13:14-25. *See also Mailloux* at 2:1-25; 3:39-4:10; 5:1-7; 6:24-50; 9:56-10:7; 11:19-30; 12:5-17; 12:26-32; 12:33-54; 19:50-59; FIG. 7; FIG. 8; FIG. 19. To the extent that the preamble is limiting and is not disclosed, either explicitly or inherently, by *Mailloux*, this limitation is obvious in combination with the knowledge of one of skill in the art and/or it would have been obvious to one of skill in the art at the time of the '417 patent to combine this reference with any of the other references in Appendix C as charted for this claim limitation. The motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
1[a] a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;	The Court has not yet construed the claims and therefore the meaning of the terms in the claims has yet to be resolved by the Court. The support identified here for this limitation is responsive to Plaintiff's infringement contentions, which Defendants disagree with. *Mailloux* discloses a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system. *See, e.g.*,